REMARKS

Claims 1, 3-17 and 19-22 are pending in the application.

Claims 1, 3-17 and 19-22 have been rejected.

Claim 20 has been amended.

Rejections under 35 U.S.C. §103(a)

Claims 1, 3-17 and 19-22 have been rejected under 35 USC §103(a) as being unpatentable over Baxter (US Patent No. 5, 826,096) in view of Jouppi (U.S. Patent No. 5,150,469). Applicants respectfully traverse these rejections.

In rejecting claims 1 and 3, the Examiner asserts that cited reference, Baxter, does not implicitly derive register specifiers however, Jouppi teaches "incrementing appropriate register specifiers." Applicants respectfully suggest that Jouppi has been misinterpreted.

Contrary to the Examiner's position, the relied upon portions of Jouppi (col. 17, line 20), Jouppi does not disclose or suggest implicitly deriving register specifiers for executing an instruction as recited in claims 1and 3. In contrast, Jouppi describes the timing for a specific FPU ALU instruction. The Examiner will note that the FPU ALU instruction, as described by Jouppi, is executed by a floating point unit (FPU 20). FPU 20 executes FPU ALU instructions in multiple stages consisting of multiple phases as described in table X, col. 16 line 63 – col. 17 line 40.

The Examiner has cited stage WB(EX1), phase 2 of FPU ALU instruction timing when the appropriate register specifier is incremented. However, when the reference is more carefully reviewed, it is apparent that Jouppi does not execute on instruction in which a register specifier is implicitly-derived based on a register specifier of instruction that is explicitly-specified as required by claim 1. Instead, Jouppi discloses a pipeline for vector operations in which after register contents are latched for a given execution of an FPU ALU instruction and after that execution begins, register specifiers for a next execution, if any, are incremented. Applicant directs the Examiner's attention to the entirety of phase 2 and 3, stage WB(EX1) in table X of Joupi, where in addition to incrementing register specifiers (for a next execution), vector length

is decremented and subsequent executions proceed (Load WB remains asserted) if vector length remains. Notably, the incremented register specifiers do not play a role in the given execution. If at all, the incremented register specifier play a role in a next execution. Accordingly, Jouppi does not disclose o suggest execution of instruction in which a register specifier is implicitly derived, based on an explicitly-specified register specifier as required by claim 1.

Other reference of record, including Baxter, does not provide the missing disclosure. Accordingly, neither Baxter nor Jouppi, taken alone or in combination, disclose or suggests the subject matter of claim 1. Though of substantially differing scope, claim 20 (as amended) and those depending therefrom, are similarly allowable. As a result, claim 1 and 20 and those depend therefrom, are patentably distinguishable from the cited references. Applicants respectfully submit that each claim is in condition for allowance.

The Examiner has generally rejected claims 5-6 in view of the cited reference and has not provided specific reasons. Applicants respectfully request the examination of claims 5 and 6 and request the Examiner to specifically point to the sections of the cited references on which the elements of claims 5 and 6 reads upon.

In rejecting claims 8-16, the Examiner has generally cited col. 4 lines 23-24 of Baxter. Applicants do not understand the Examiner's rejection of claims 8-16 in view of the cited sections of Baxter. In the cited sections, Baxter describes a data word size (64-bit) for performing double precision floating point operation. In contrast, claims 8-16 recite specific double-precision floating point instructions and appropriate equations. Accordingly, claims 8-16 are patentably distinguishable from the cited reference. Applicants respectfully submit that claims 8-16 are in condition for allowance.

The Examiner has generally rejected claims 17 and 19-22 in view of the cited reference and has not provided specific reasons. Applicants respectfully request the examination of claims 17 and 19-22 and request the Examiner to specifically point to the sections of the cited references on which the elements of claims 17 and 19-22 reads upon.

Finally, for the record, and with all due respect, Applicant notes that Examiner's observations with respect to claims 5-6, 8-17 and 19-22, none of the limitations of these claims

have been considered. Applicants respectfully request allowance or, in alternative, substantive examination of these claims.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

Michael P. Noonan — July 30, 2002 (Date)

Respectfully submitted,

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MARKED-UP COPY OF AMENDED CLAIMS IN ACCORDANCE WITH 37 C.F.R. § 121(c)(ii)

20. (Amended) A method of operating a processor comprising:

storing information in a register file including a plurality of registers;

executing instructions in a functional unit coupled to the register file and operating upon a plurality of registers in the register file;

explicitly defining a register specifier of a register operated upon during executing of the instruction; and

implicitly deriving a register specifier **of a register operated upon during executing of the instruction** based on the explicitly defined register specifier.